A Recursive Structure Power Aware Imprecise Multiplier

By Eric Zhang & Xinfei Guo

Problem Statement (Motivation)

- Multiplier is one of the most basic and important components in today digital computing systems
- However, multipliers often consume large percentage of total power
- Traditional Methods such as dynamic voltage scaling, power and clock gating are limited by technologies and accuracy

Problem Statement (Motivation)

- Many digital applications such as multimedia, DSP and some communications does not require 100% accuracy
- Relax accuracy requirement for trade off with power and performance

Related Work

- Mark S. K. Lau, Keck-Voon Ling,etc.

  - An energy-aware probabilistic multiplier
- Jiun-Ping Wang, Shiann-Rong Kuang

  - A low-power reconfigurable signed pipeline array multiplier
- Chip-Hong Chang, Ravi Kumar Satzoda

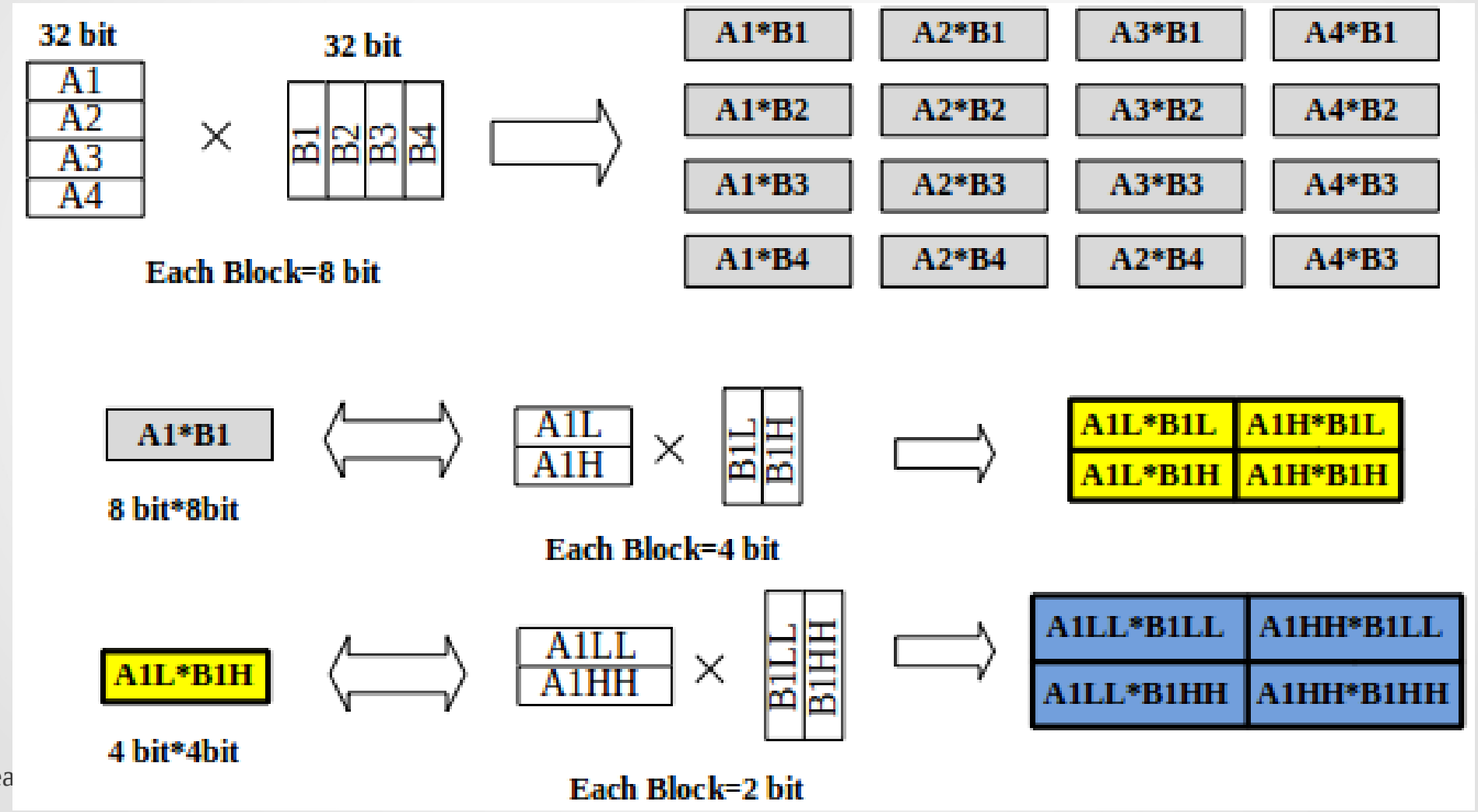
  - a novel multiplexer based truncated array multiplier
- Zhijun Huang

  - a left-to-right array multiplier

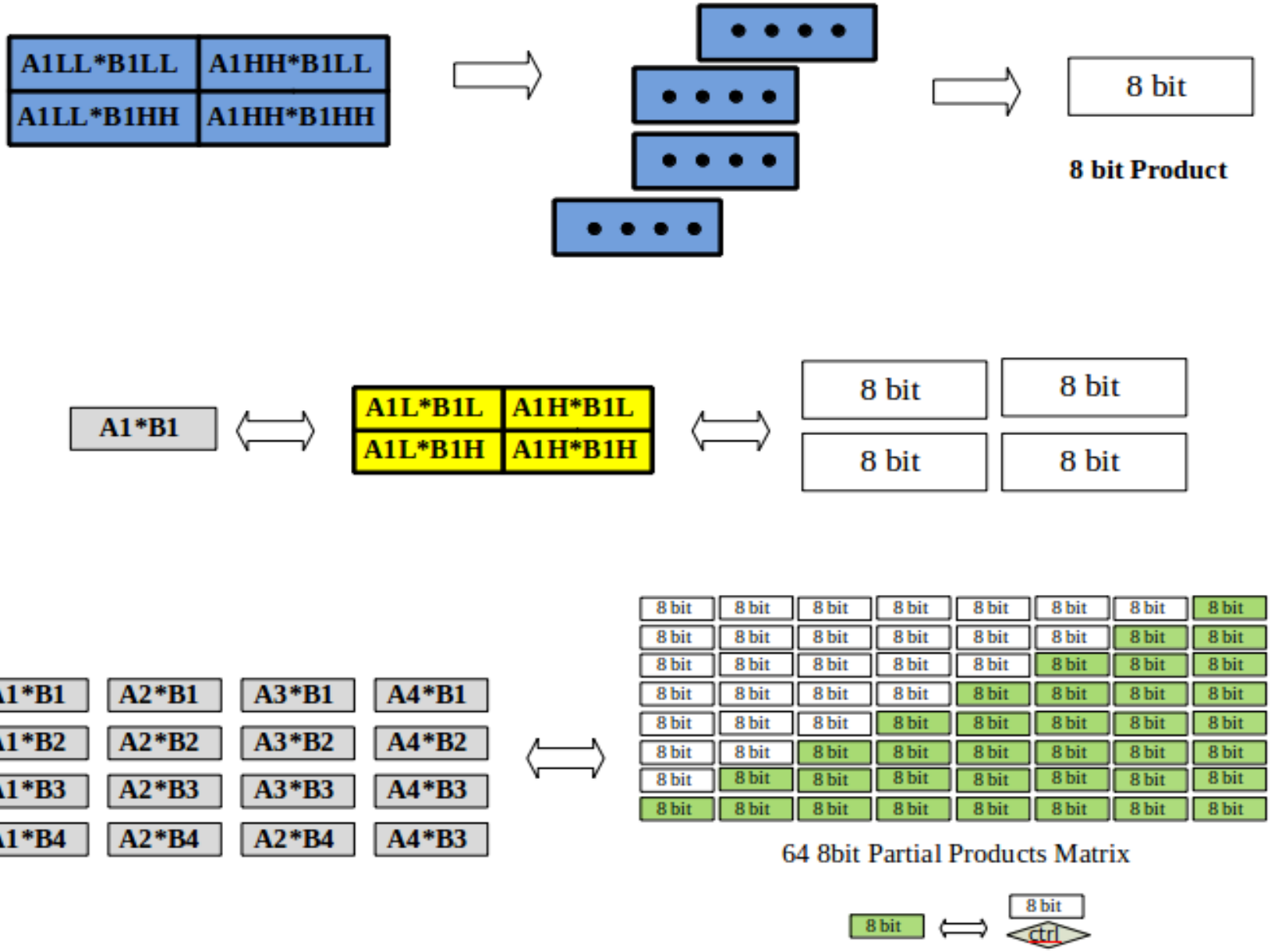
Our design of the new multiplier: PABITM

- A recursive structure power aware imprecise multiplier
- A novel design incorporates both array and tree structure
- Block based array structure allows finer control on precision
- Introduce fidelity as an additional design knob
- New Pareto optimal curve/surface

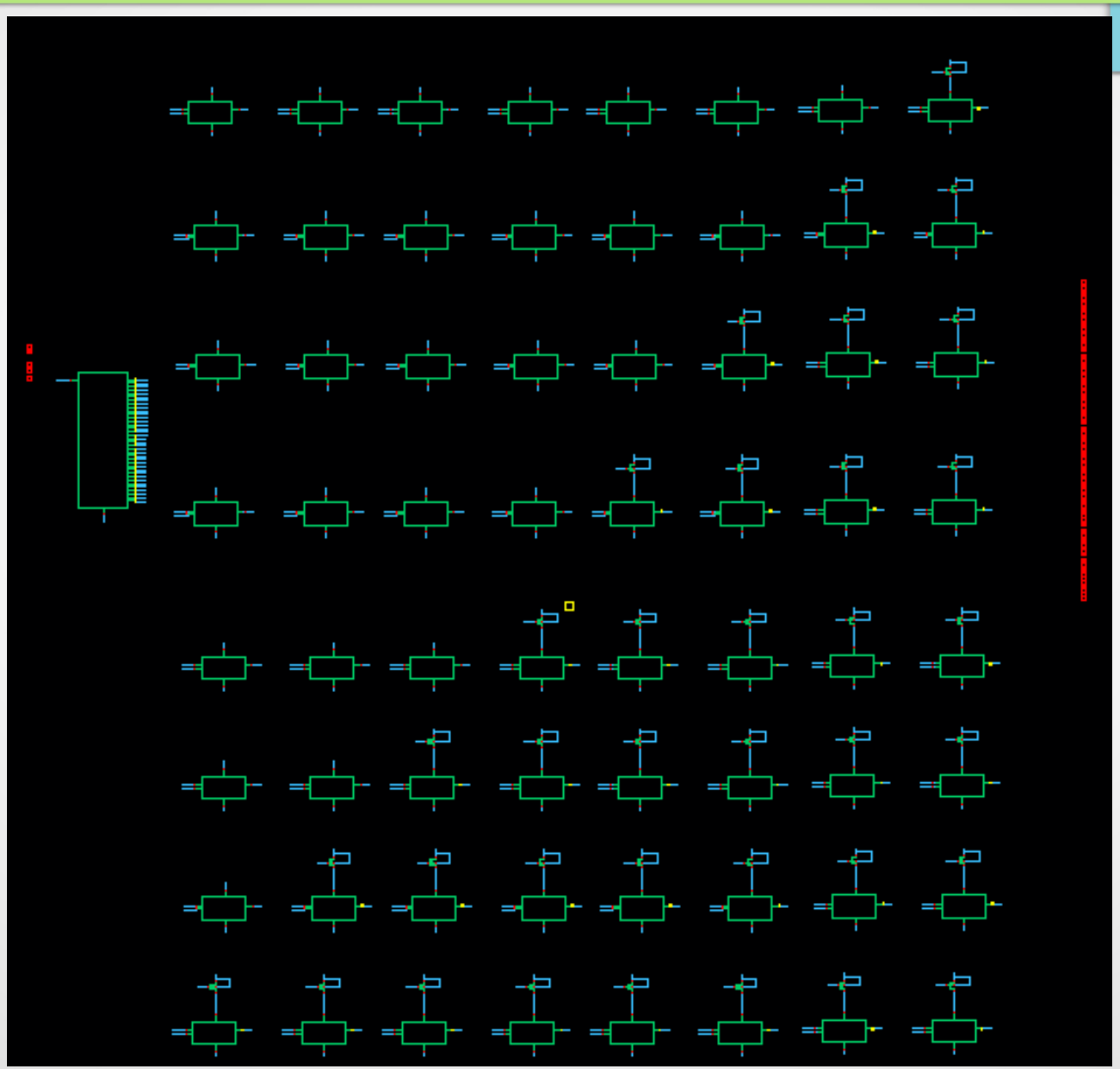
PABITM: Architecture



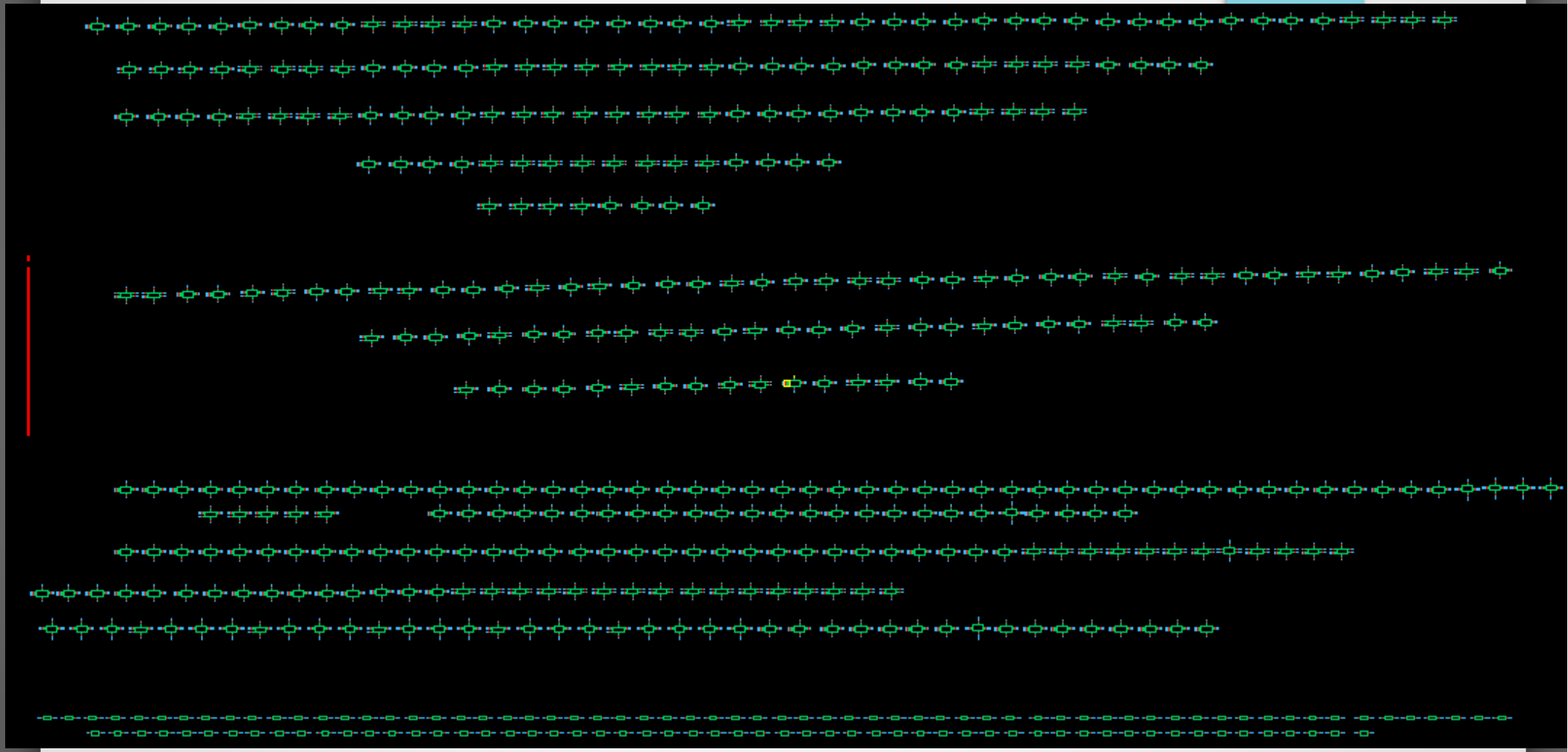
PABITM: Architecture



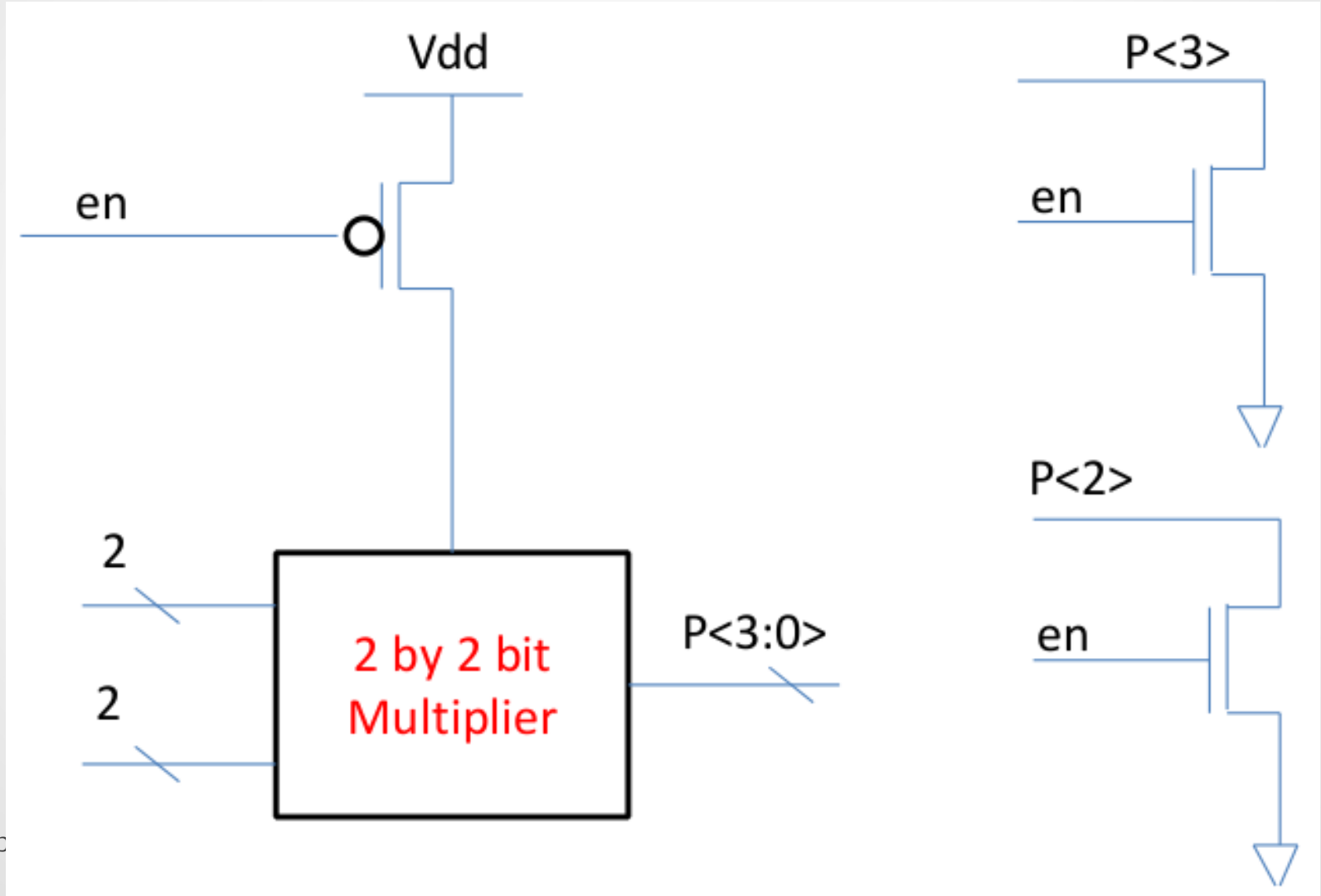
Block Array Multiplication



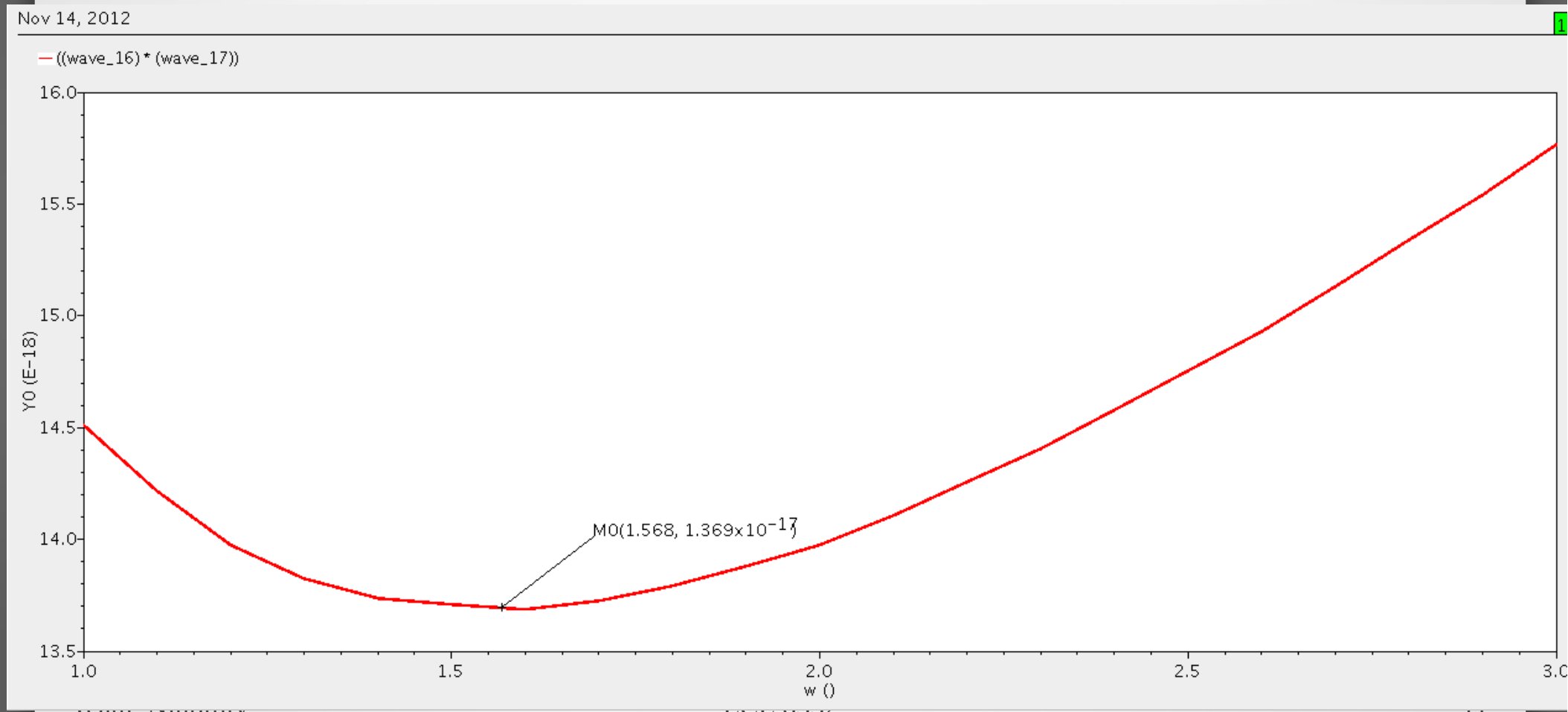
Tree Accumulation Circuit



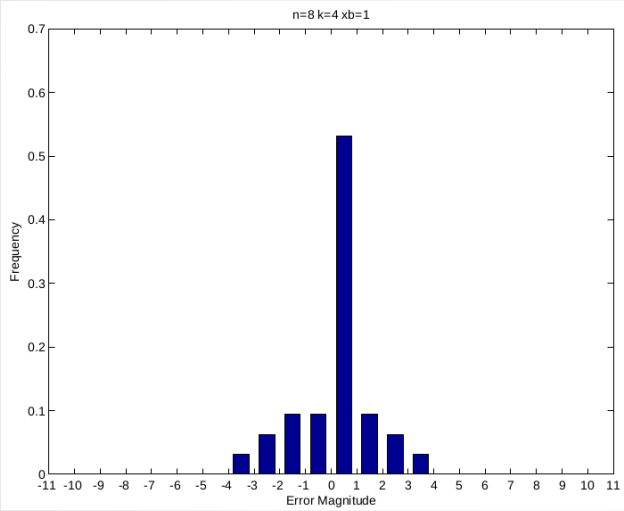
PABITM: Power Gating (imprecise technique)

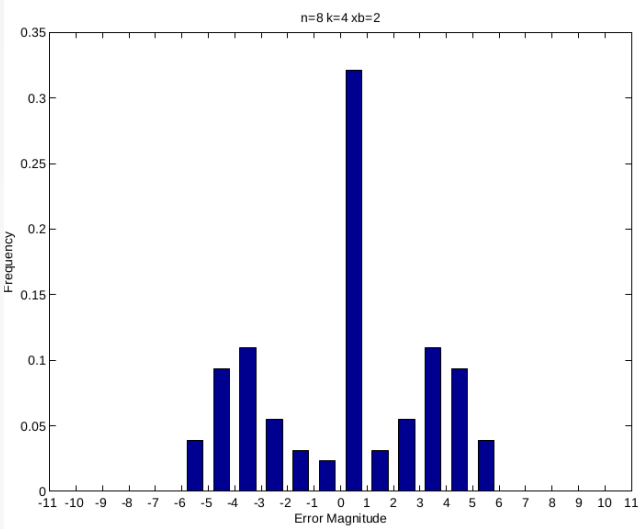


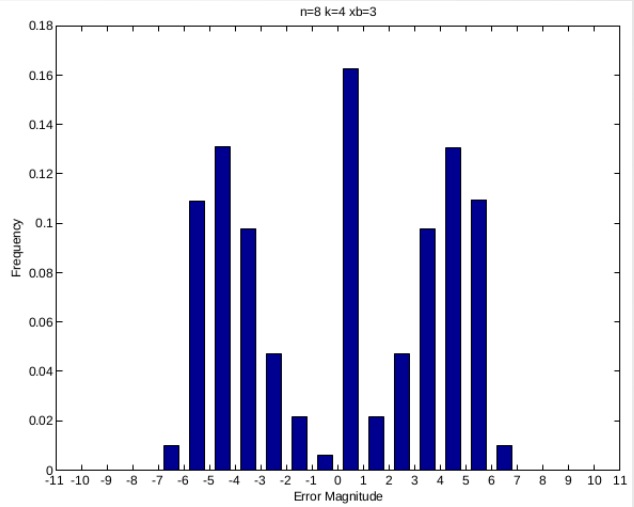
Sizing (Power and Delay Optimization)

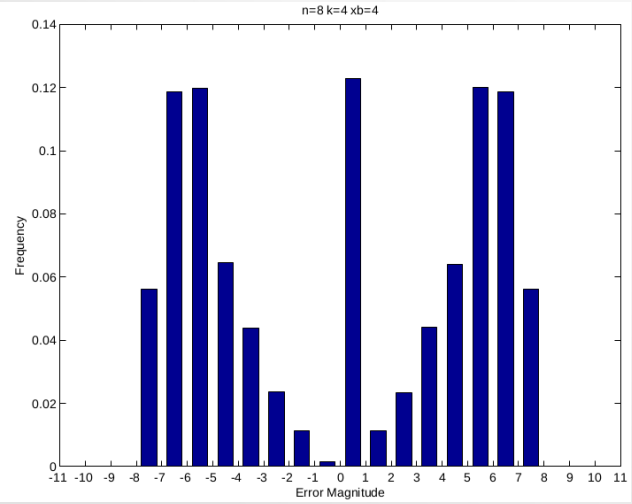


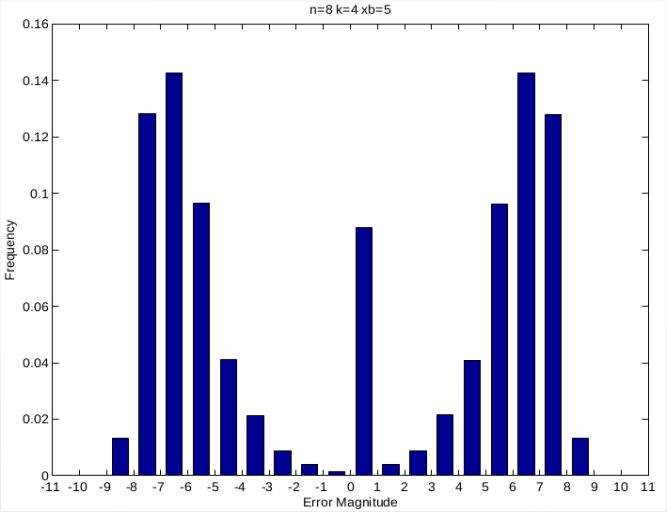
Error Characterization

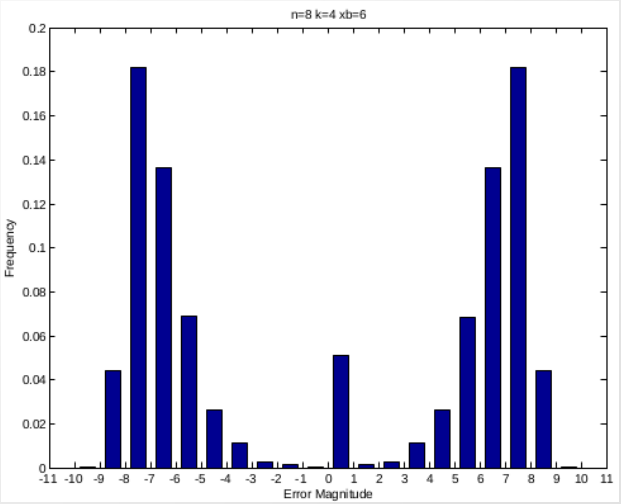




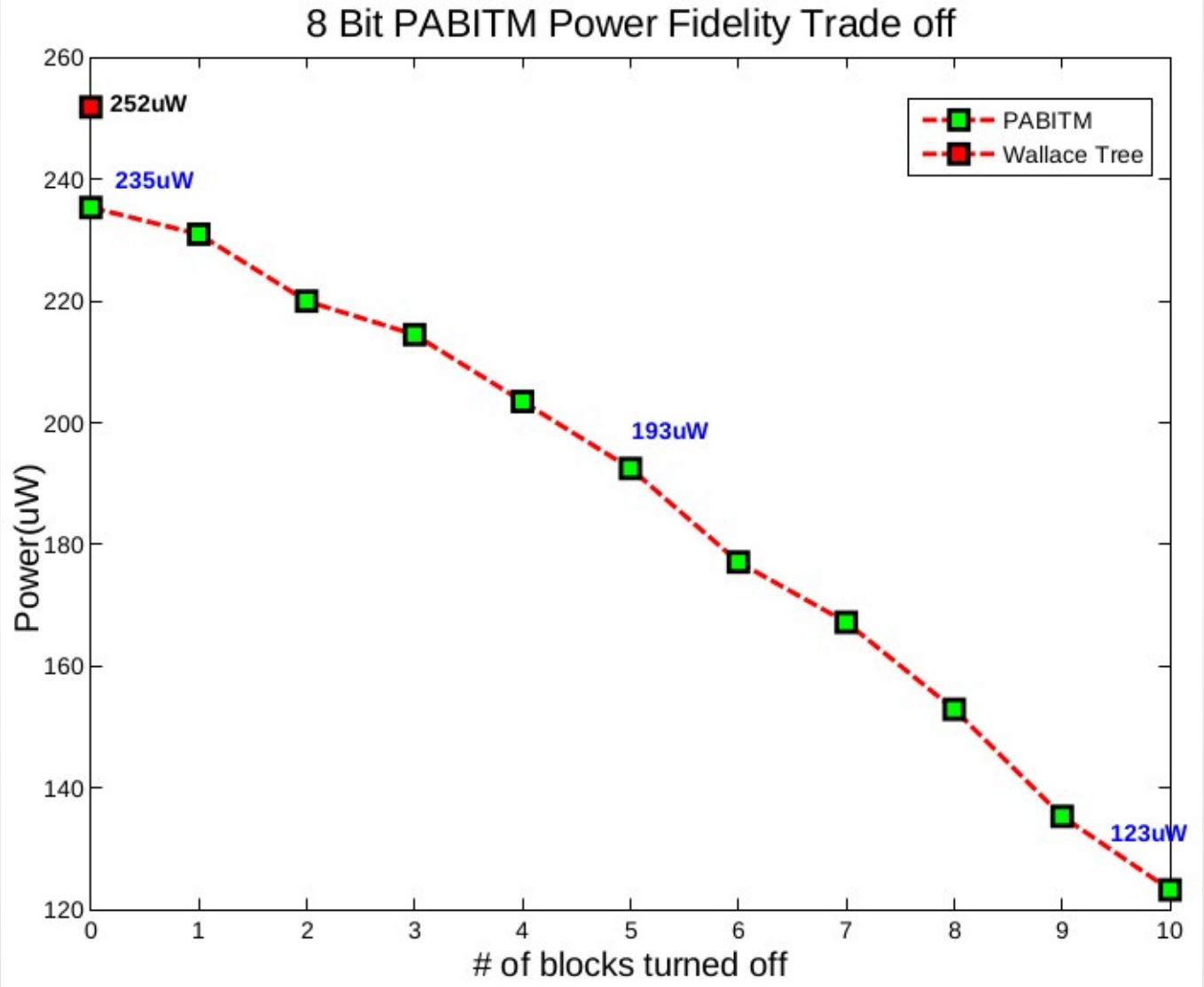




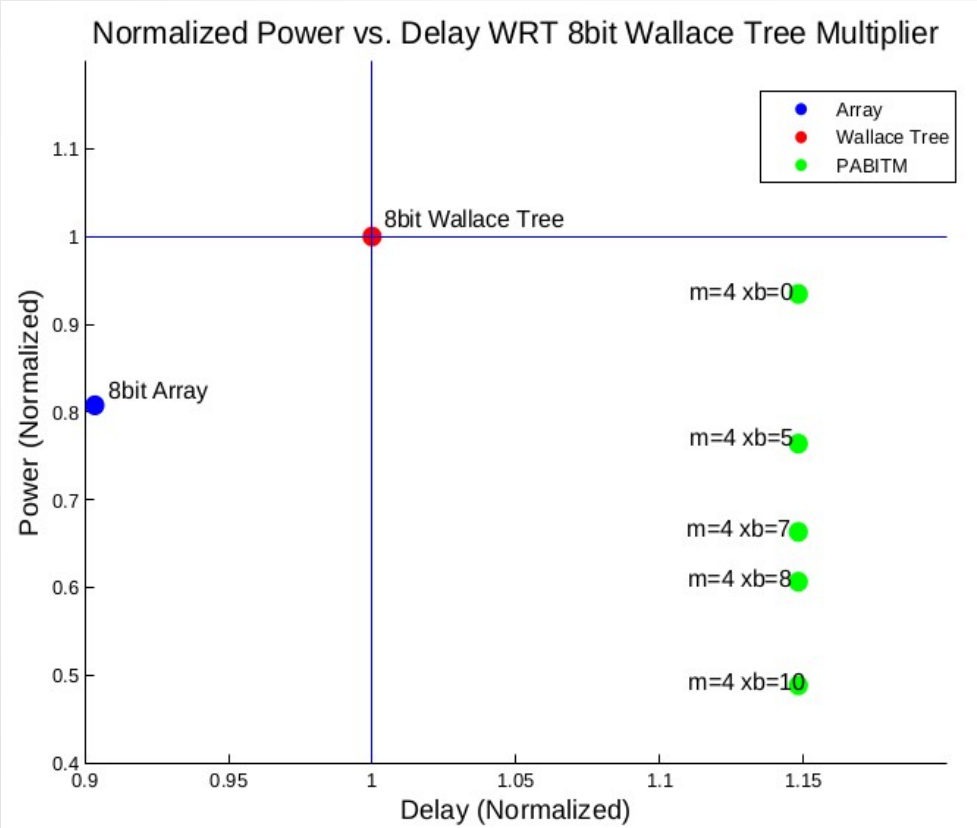


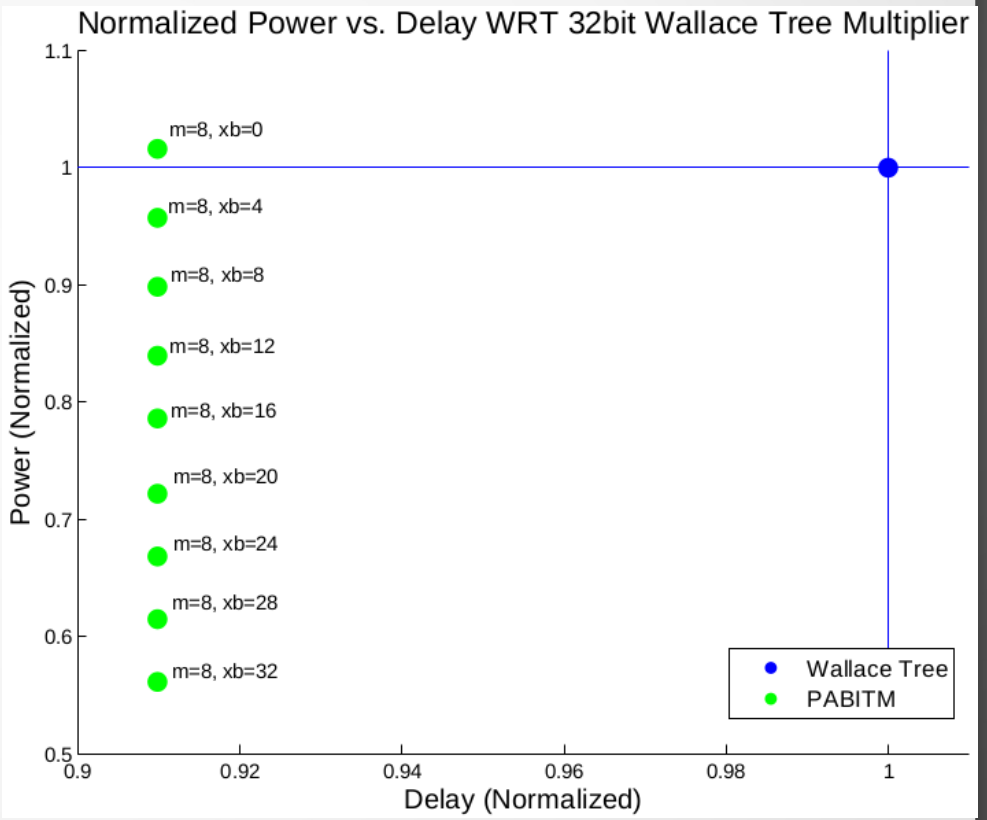


8bit PABITM Power Fidelity Trade off



Simulation Results





JPEG Case Study

Xb = 0
ssim = 1

Xb =12
ssim = 0.82

Xb = 20
ssim = 0.7

Xb = 30
ssim = 0.7

Conclusion

- Up to 47% power savings and 10% performance improvement for a 32 bit multiplier compared to the Wallace Tree
- Small area overhead
- JPEG case study shows that the PABITM can be well used by the JPEG compression algorithm

Future Work

- Compare to state of art designs that employs other techniques
- Use imprecise adder as the final stage accumulation adder to speed up performance
- Explore the effect of different block sizes on power and performance
- Extend this architecture to floating point multipliers

Contributions

- Eric:
  - Architecture design
  - 8 bit Array multiplier implementation
  - 32 bit PABITM implementation
  - Power and delay simulation
- Xinfei:
  - 8 bit PABITM implementation
  - Power gating
  - Zero detection
  - 32 bit Wallace Tree implementation